

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

### Description

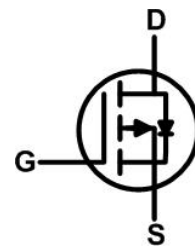
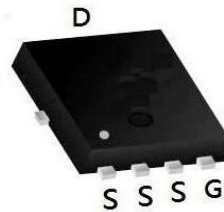
The XXW50P03DF is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The XXW50P03DF meet the RoHS and Gree Product requirement 100% EAS guaranteed with full function reliability approved.

### Product Summary

BVDSS	RDSON	ID
-30V	8.7mΩ	-50A

### PRPAK5X6 Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V <sub>DS</sub>	Drain-Source Voltage	-30		V
V <sub>GS</sub>	Gate-Source Voltage	±25		V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	-50		A
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	-32		A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	-150		A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	125		mJ
I <sub>AS</sub>	Avalanche Current	-50		A
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>4</sup>	5	2.0	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150		°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150		°C

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	°C/W

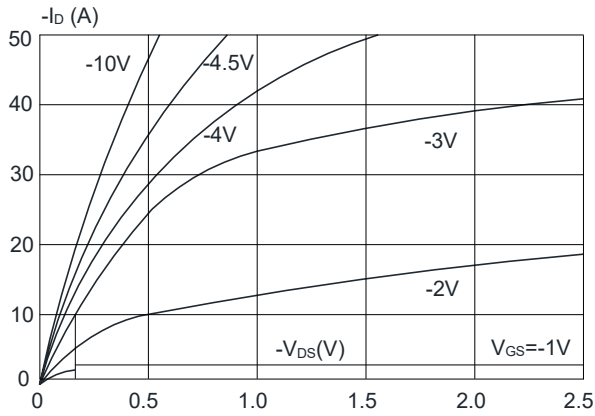
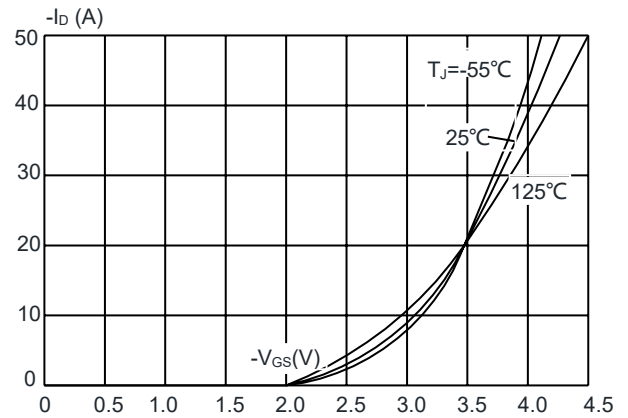
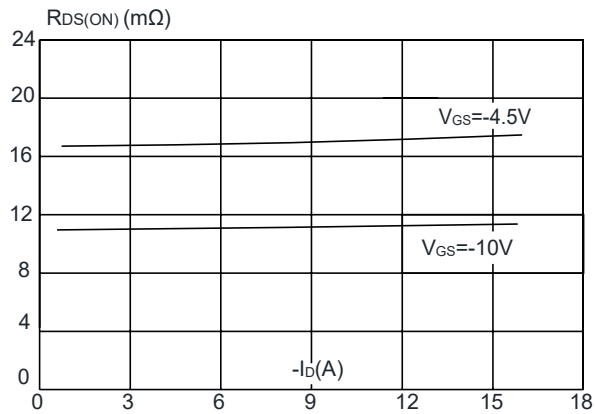
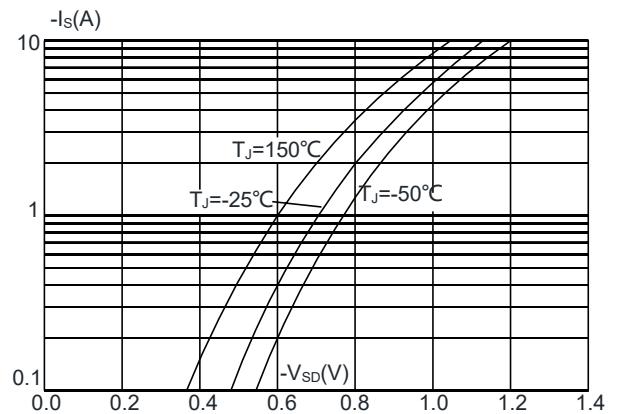
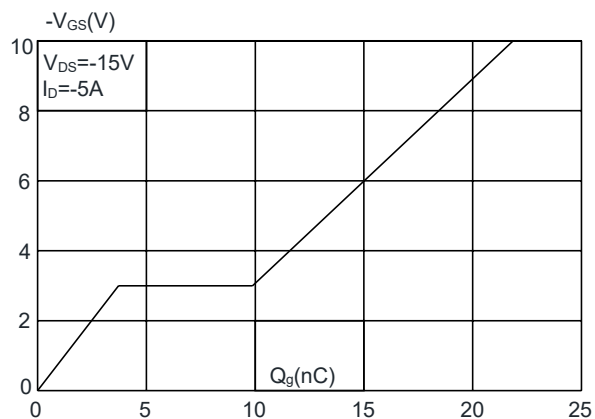
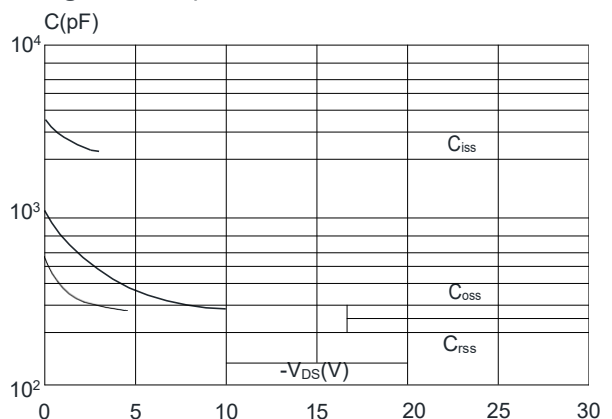
**Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$  unless otherwise specified)

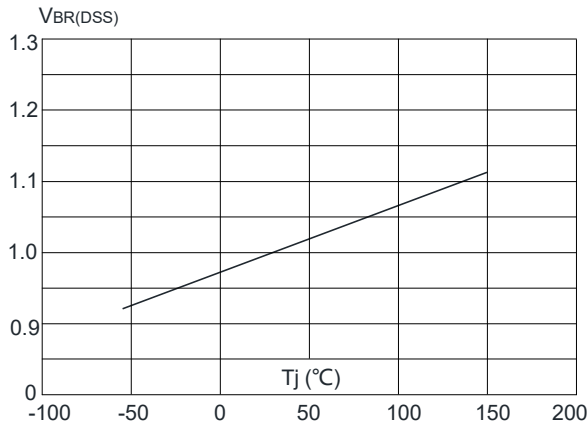
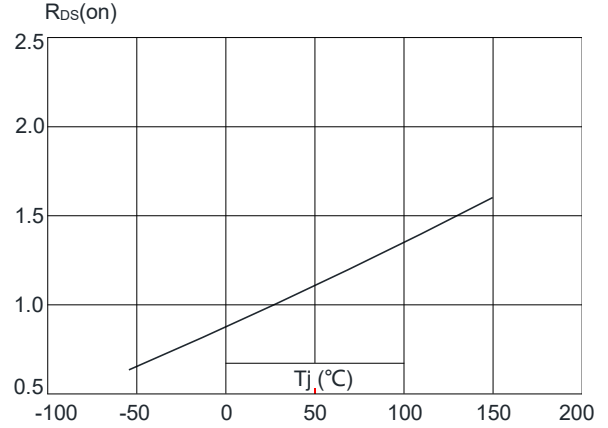
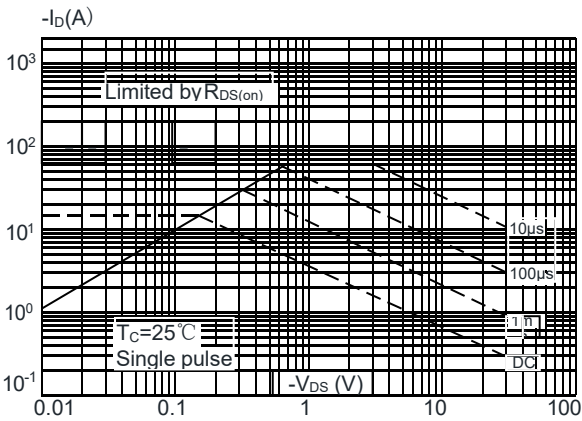
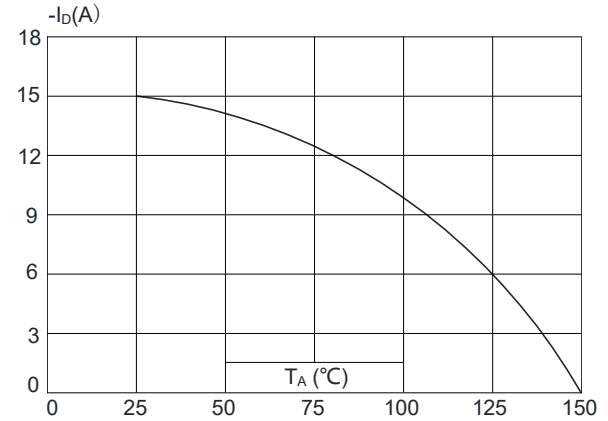
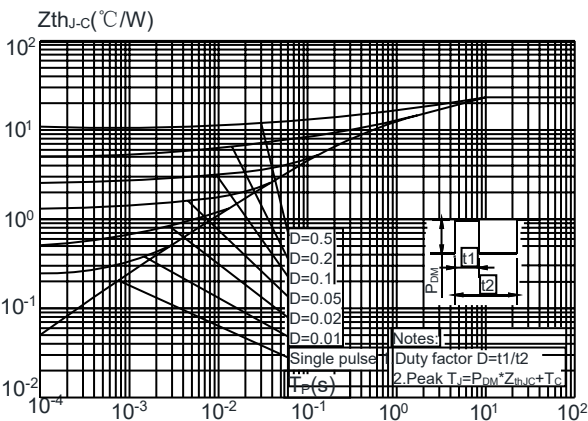
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-30V, V_{GS}=0V,$	-	-	-1	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.6	-2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance Note3	$V_{GS}=-10V, I_D=-10A$	-	8.7	14	m $\Omega$
		$V_{GS}=-4.5V, I_D=-5A$	-	17	24	
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V,$ $f=1.0MHz$	-	1770	-	pF
$C_{oss}$	Output Capacitance		-	233	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	206	-	pF
$Q_g$	Total Gate Charge	$V_{DS}=-15V, I_D=-5A,$ $V_{GS}=-10V$	-	22	-	nC
$Q_{gs}$	Gate-Source Charge		-	1.0	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	1.8	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=-15V, I_D=-10A,$ $V_{GS}=-10V, R_{GEN}=2.5\Omega$	-	9	-	ns
$t_r$	Turn-on Rise Time		-	13	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	48	-	ns
$t_f$	Turn-off Fall Time		-	20	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	-15	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-60	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=-15A$	-	-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$T_J=25^{\circ}\text{C},$	-	64	-	ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD}=-24V, I_F=-2.8A,$ $di/dt=-100A/\mu s$	-	25	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition:  $T_J=25^{\circ}\text{C}, V_{GS}=10V, R_G=25\Omega, L=0.5mH, I_{AS}=-12.7A$

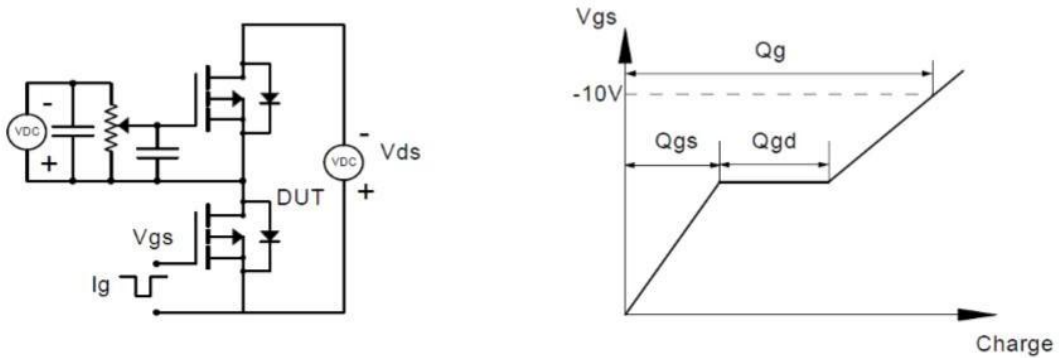
3. Pulse Test: Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 0.5\%$

**Typical Performance Characteristics**
**Figure 1: Output Characteristics**

**Figure 2: Typical Transfer Characteristics**

**Figure 3: On-resistance vs. Drain Current**

**Figure 4: Body Diode Characteristics**

**Figure 5: Gate Charge Characteristics**

**Figure 6: Capacitance Characteristics**


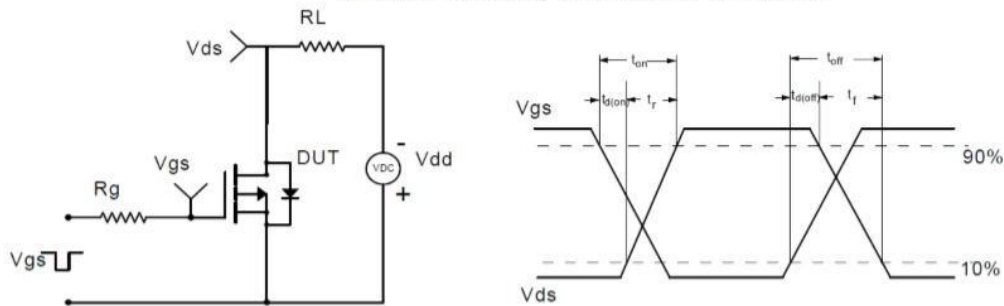
**P-Ch 30V Fast Switching MOSFETs**
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**

**Figure 8: Normalized on Resistance vs. Junction Temperature**

**Figure 9: Maximum Safe Operating Area**

**Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature**

**Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case**


**Test Circuit**

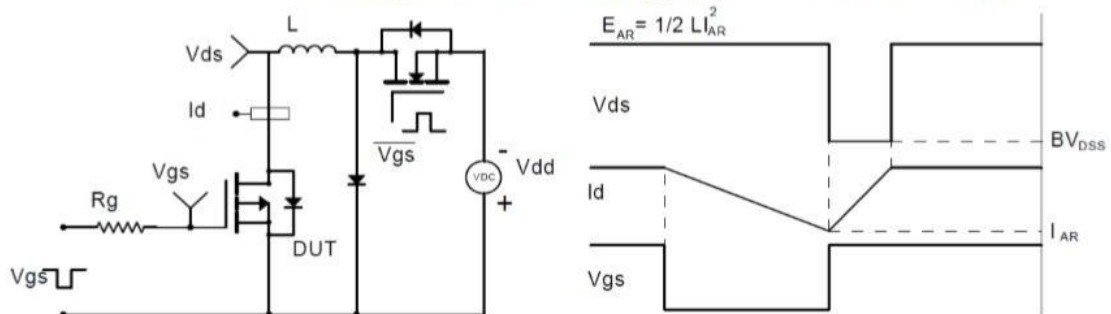
Gate Charge Test Circuit & Waveform



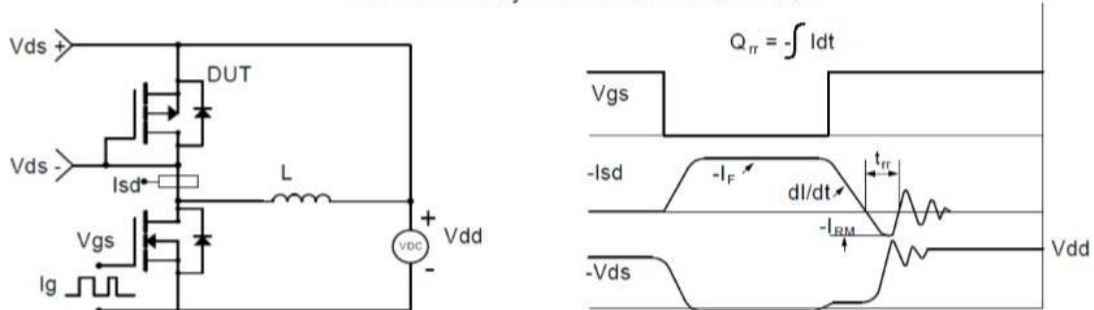
Resistive Switching Test Circuit & Waveforms

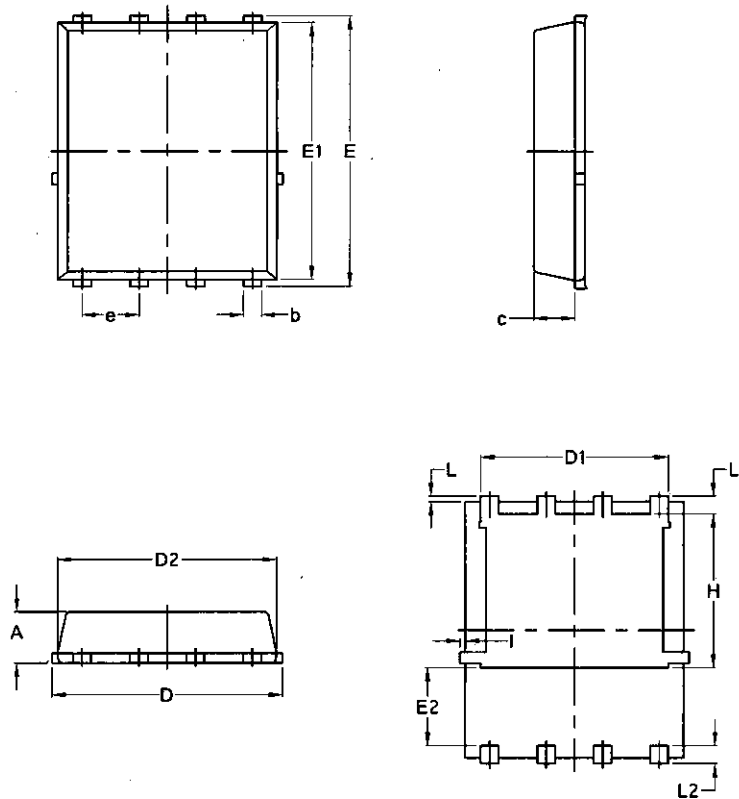


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



**Package Mechanical Data-DFN5\*6-8L-JQ Single**


Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070