

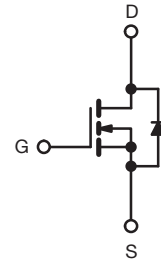
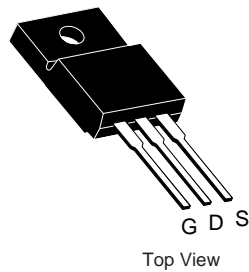
N-Channel 700 V(D-S) Power MOSFET


RoHS
 COMPLIANT

| PRODUCT SUMMARY | |
|---|------------------------------|
| V_{DS} (V) | 700 |
| $R_{DS(on)}$ max. (Ω) at 25 °C | $V_{GS} = 10\text{ V}$ 1.4 |
| Q_g Typ. (nC) | 24 |
| Q_{gs} (nC) | 6 |
| Q_{gd} (nC) | 11 |
| Configuration | Single |

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC

TO-220 FULLPAK



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | |
|---|------------------|-----------------------------------|---------------------|
| PARAMETER | SYMBOL | LIMIT | UNIT |
| Drain-source voltage | V_{DS} | 700 | V |
| Gate-source voltage | V_{GS} | ± 30 | |
| Continuous drain current ($T_J = 150\text{ }^\circ\text{C}$) ^e | V_{GS} at 10 V | $T_C = 25\text{ }^\circ\text{C}$ | A |
| | | $T_C = 100\text{ }^\circ\text{C}$ | |
| Pulsed drain current ^a | I_{DM} | 18 | |
| Linear derating factor | | 0.63 | W/ $^\circ\text{C}$ |
| Single pulse avalanche energy ^b | E_{AS} | 56 | mJ |
| Maximum power dissipation | P_D | 31 | W |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Drain-source voltage slope | dV/dt | $T_J = 125\text{ }^\circ\text{C}$ | V/ns |
| Reverse diode dV/dt ^d | | 27 | |
| Soldering recommendations (peak temperature) ^c | For 10 s | 300 | $^\circ\text{C}$ |
| Mounting torque | M3 screw | 0.6 | Nm |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 28.2\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2\text{ A}$
- 1.6 mm from case
- $I_{SD} \leq I_D$, $dI/dt = 100\text{ A}/\mu\text{s}$, starting $T_J = 25\text{ }^\circ\text{C}$
- Limited by maximum junction temperature

| THERMAL RESISTANCE RATINGS | | | | |
|-----------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum junction-to-ambient | R_{thJA} | 43 | 65 | °C/W |
| Maximum junction-to-case (drain) | R_{thJC} | 3.1 | 4.0 | |

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|--|---------------------|---|---|------|------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 700 | - | - | V |
| V_{DS} temperature coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | | - | 0.73 | - | V/°C |
| Gate-source threshold voltage (N) | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2 | - | 4 | V |
| Gate-source leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| | | $V_{GS} = \pm 30\text{ V}$ | | - | - | ± 1 | μA |
| Zero gate voltage drain current | I_{DSS} | $V_{DS} = 700\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 1 | μA |
| | | $V_{DS} = 560\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 10 | |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 3\text{ A}$ | - | 1.36 | - | Ω |
| Forward transconductance | g_{fs} | $V_{DS} = 30\text{ V}, I_D = 3\text{ A}$ | | - | 2 | - | S |
| Dynamic | | | | | | | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$ | | 410 | 820 | - | pF |
| Output capacitance | C_{oss} | | | 20 | 60 | - | |
| Reverse transfer capacitance | C_{rss} | | | 2 | 4 | - | |
| Effective output capacitance, energy related ^a | $C_{o(er)}$ | $V_{DS} = 0\text{ V to } 560\text{ V}, V_{GS} = 0\text{ V}$ | | - | 36 | - | |
| Effective output capacitance, time related ^b | $C_{o(tr)}$ | | | - | 117 | - | |
| Total gate charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 3\text{ A}, V_{DS} = 520\text{ V}$ | - | 24 | 48 | nC |
| Gate-source charge | Q_{gs} | | | - | 6 | - | |
| Gate-drain charge | Q_{gd} | | | - | 11 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 560\text{ V}, I_D = 3\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$ | | - | 14 | 28 | ns |
| Rise time | t_r | | | - | 12 | 24 | |
| Turn-off delay time | $t_{d(off)}$ | | | - | 30 | 60 | |
| Fall time | t_f | | | - | 20 | 40 | |
| Gate input resistance | R_g | $f = 1\text{ MHz}, \text{open drain}$ | | 0.4 | 1.4 | 2.7 | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous source-drain diode current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 7 | A |
| Pulsed diode forward current | I_{SM} | | | - | - | 18 | |
| Diode forward voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 3\text{ A}, V_{GS} = 0\text{ V}$ | | - | 0.83 | 1.3 | V |
| Reverse recovery time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$ | | 118 | 237 | 474 | ns |
| Reverse recovery charge | Q_{rr} | | | - | 2.2 | - | μC |
| Reverse recovery current | I_{RRM} | | | - | 16 | - | A |

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

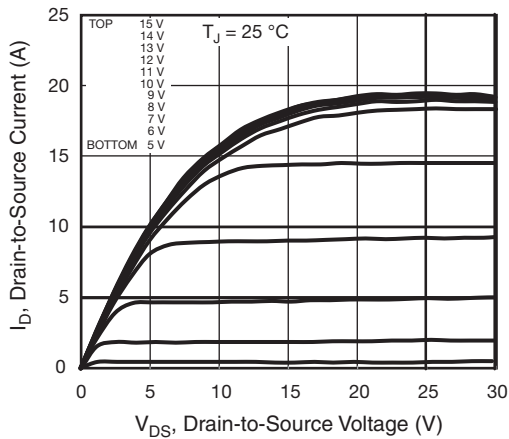


Fig. 1 - Typical Output Characteristics

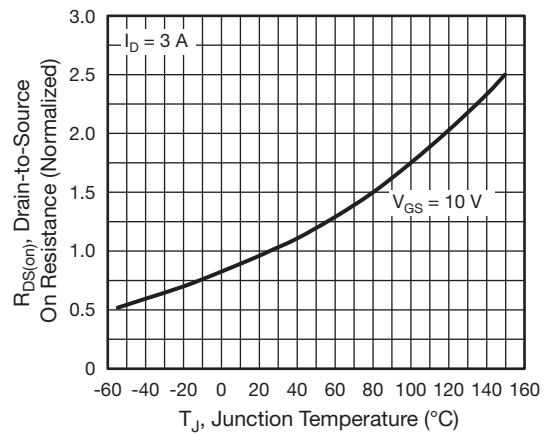


Fig. 4 - Normalized On-Resistance vs. Temperature

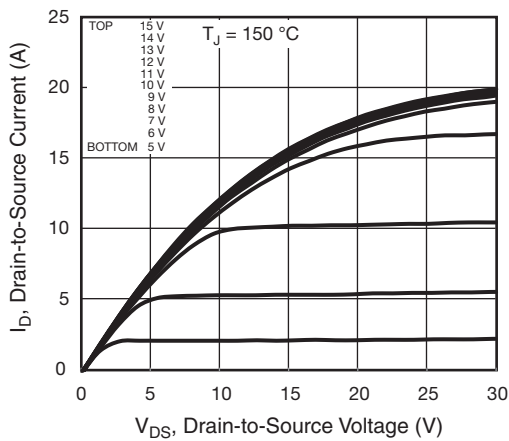


Fig. 2 - Typical Output Characteristics

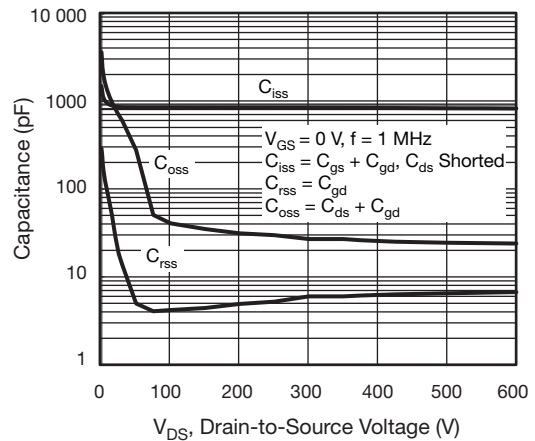


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

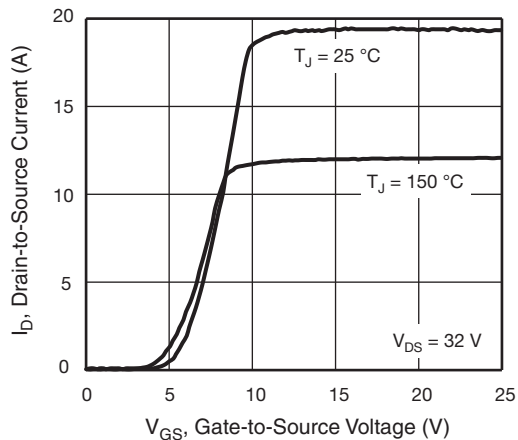


Fig. 3 - Typical Transfer Characteristics

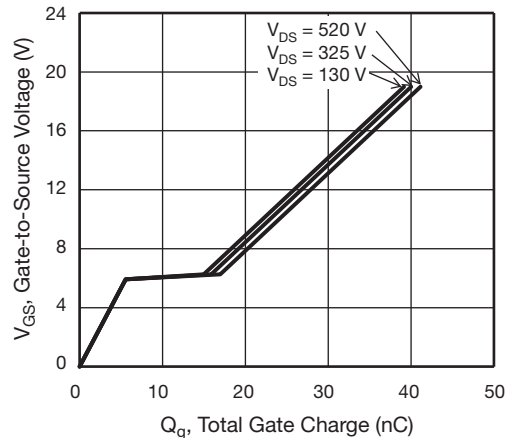


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

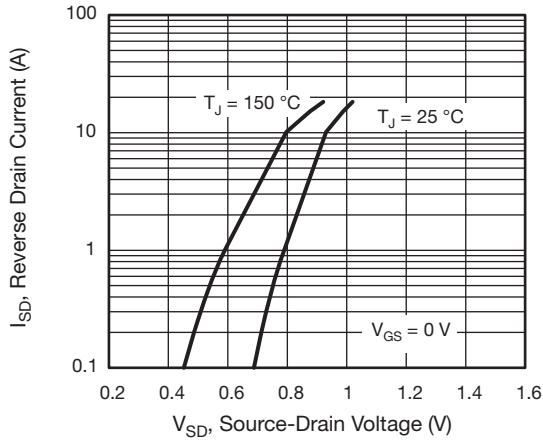


Fig. 7 - Typical Source-Drain Diode Forward Voltage

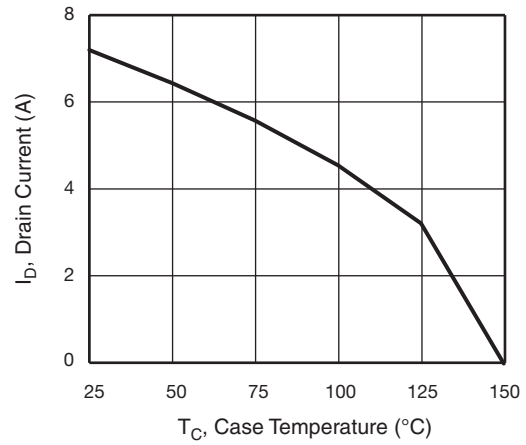


Fig. 9 - Maximum Drain Current vs. Case Temperature

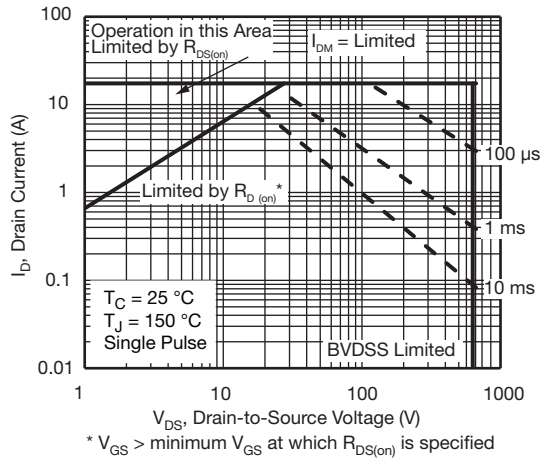


Fig. 8 - Maximum Safe Operating Area

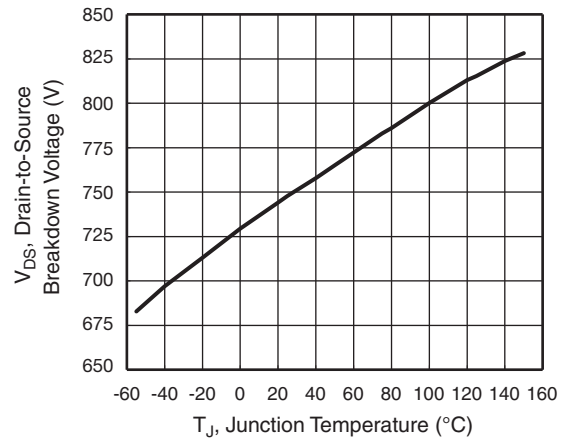


Fig. 10 - Temperature vs. Drain-to-Source Voltage

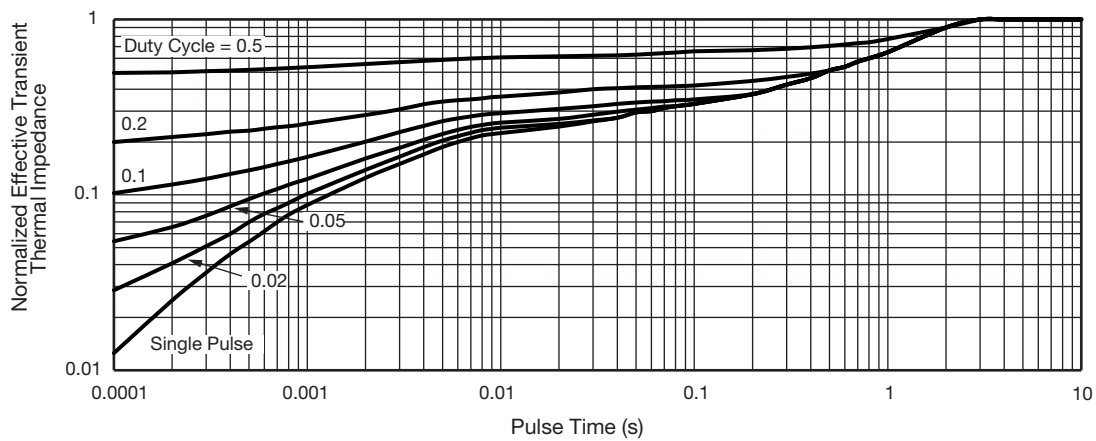


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

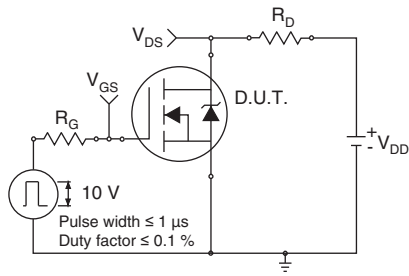


Fig. 12 - Switching Time Test Circuit

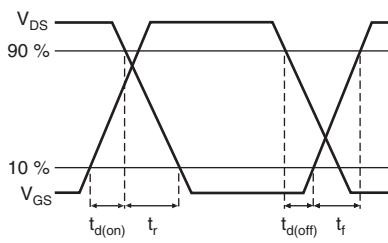


Fig. 13 - Switching Time Waveforms

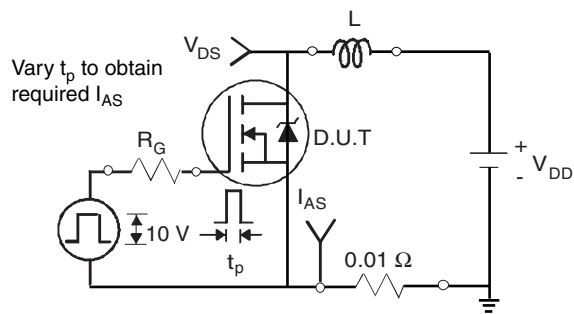


Fig. 14 - Unclamped Inductive Test Circuit

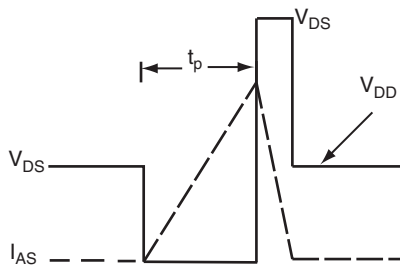


Fig. 15 - Unclamped Inductive Waveforms

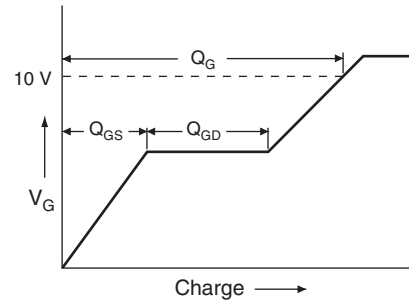


Fig. 16 - Basic Gate Charge Waveform

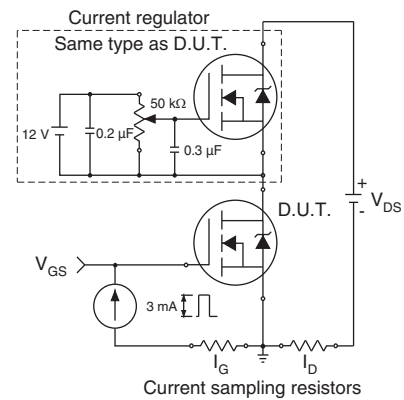
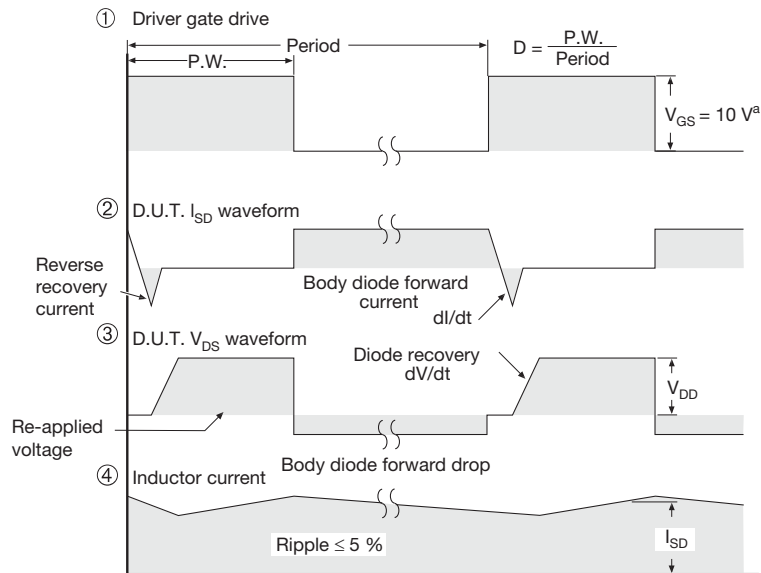
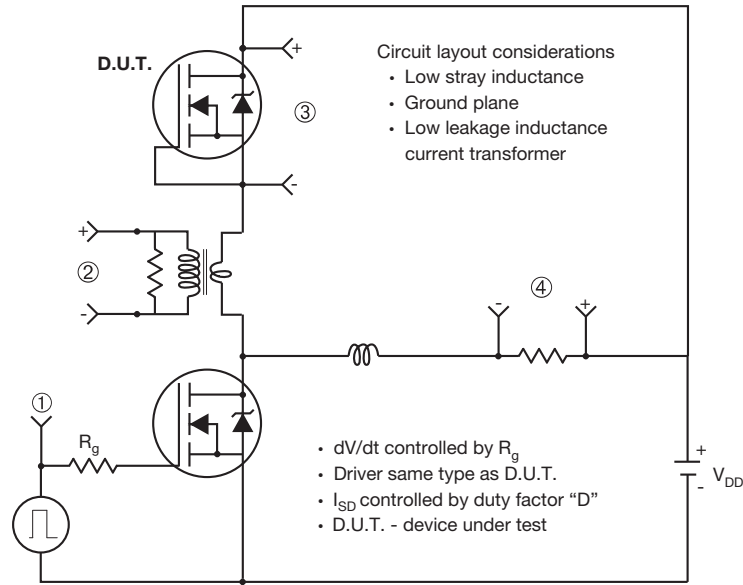


Fig. 17 - Gate Charge Test Circuit

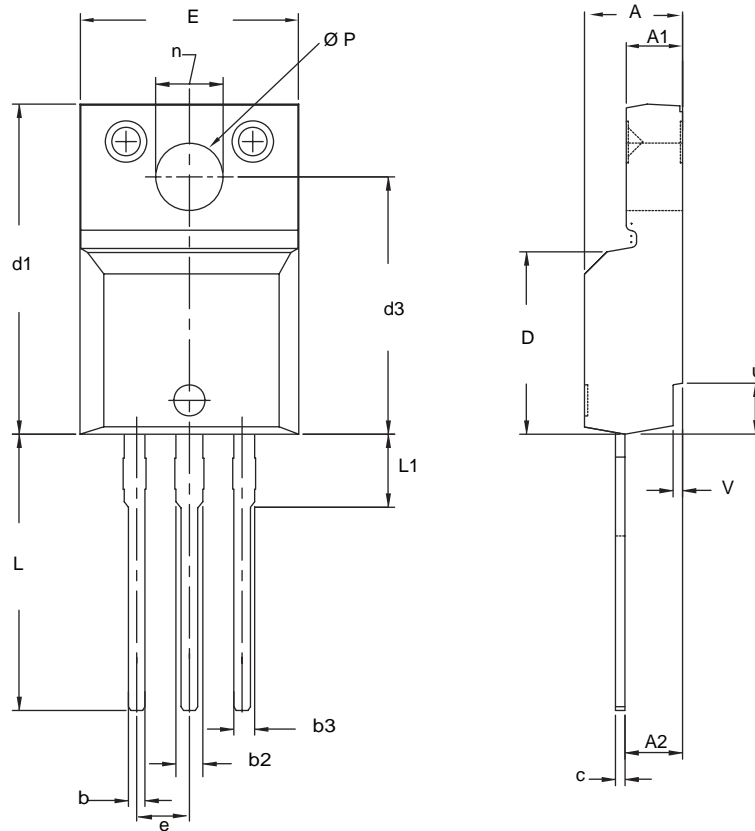
Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

TO-220 FULLPAK (HIGH VOLTAGE)


| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|--------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.570 | 4.830 | 0.180 | 0.190 |
| A1 | 2.570 | 2.830 | 0.101 | 0.111 |
| A2 | 2.510 | 2.850 | 0.099 | 0.112 |
| b | 0.622 | 0.890 | 0.024 | 0.035 |
| b2 | 1.229 | 1.400 | 0.048 | 0.055 |
| b3 | 1.229 | 1.400 | 0.048 | 0.055 |
| c | 0.440 | 0.629 | 0.017 | 0.025 |
| D | 8.650 | 9.800 | 0.341 | 0.386 |
| d1 | 15.88 | 16.120 | 0.622 | 0.635 |
| d3 | 12.300 | 12.920 | 0.484 | 0.509 |
| E | 10.360 | 10.630 | 0.408 | 0.419 |
| e | 2.54 BSC | | 0.100 BSC | |
| L | 13.200 | 13.730 | 0.520 | 0.541 |
| L1 | 3.100 | 3.500 | 0.122 | 0.138 |
| n | 6.050 | 6.150 | 0.238 | 0.242 |
| ØP | 3.050 | 3.450 | 0.120 | 0.136 |
| u | 2.400 | 2.500 | 0.094 | 0.098 |
| v | 0.400 | 0.500 | 0.016 | 0.020 |

ECN: X09-0126-Rev. B, 26-Oct-09
 DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.